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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/722,249	11/22/2000	Guang Yang	06618-560001/CIT-3124	3955

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EXAMINER	
NAKHJAVAN, SHERVIN K	

ART UNIT	PAPER NUMBER
2621	

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7

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/722,249	YANG ET AL.	
	Examiner	Art Unit	
	Shervin Nakhjavan	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,12 and 14-18* is/are rejected.

7)☒ Claim(s) *9-11 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8, 12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elabd et al. (US 5,196,939) in view of Cho (US 6,166,367).

Regarding claims 1-8, 12 and 14-18, Elabd teaches, limitation of claim 1, a vision system (Column 3, Lines 60-66, where system of figure 1 is the vision system), comprising: a pixel array having an array of pixels, said array of pixels configured to receive light signals from an image having at least on tracking target (Column 4, Lines 12-17, where the image array produced from a camera i.e. a ccd is the pixel array receiving light signals from an image as discussed with respect to figure 2A, regarding the tracking target, Column 4, Lines 6-11); at least one multi-resolution window operation circuit configured to process said image, each of said at least one multi-resolution window operation circuit operating to process each of said at least one tracking target within a particular multi-resolution window (Column 4, Lines 6-11, where a window operation is performed based on the selected tracking target i.e. the airplane of figure 2B within a selected rows and columns which make the windowing operation for segmenting the image of the plane from the initial image and in addition the operation can be multi resolution based on spatial filtering of the image as discussed in Column 7, Lines 40-55, wherein the amount of resolution in the image can be reduced

i.e. when objective is target tracking and enhanced when objective is target detection, Column 3, Lines 9-11);

Limitation of claim 2, the system further comprising: a target detection circuit configured to receive and process said image such that each of said at least one tracking target is assigned to said particular multi-resolution window (Column 4, Lines 6-11, where the window in figure 2B is assigned to the target airplane by assigning the rows and columns of the window area inherently);

Limitation of claim 5, system further comprising: at least one output analog signal chain, each of said at least one output analog signal chain configured to output signal from said particular multi-resolution window (Column 4, Lines 28-61, where the output port 19 outputs the chain or serially registered row data of selected columns in the registers 17A and 17B);

Limitation of claim 6, system further comprising: a plurality of latches, each latch configured to hold definition values of said particular multi-resolution window (Column 4, Lines 42-43, where the registers 17A and 17 B are the latches to hold the pixel definition of the selected rows of the window for outputting to video receiver);

Limitation of claim 7, each of said array pixels includes a poly-pixel gate biased in deep-depletion (Column 5, Lines 51-53);

Limitation of claim 12, the system further comprising: row and column control circuits operating to appropriately arrange said light signal received by said pixel array (Column 4, Lines 12-22);

Limitation of claim 14, a method for searching and tracking targets, comprising: receiving light signals from an image having at least one tracking target (Column 3, Line 60 through Column 4, Line 12, wherein the tracking target is the airplane); detecting and

separating said at least one tracking target into at least one region of interest (Column 4, Lines 6-11, wherein the image of the airplane is detected by a user and separated or windowed by the user from the rest of the image); grouping each of said at least one region of interest into a plurality of blocks (Column 4, lines 6-11, where the selected or separated object is inherently grouped by it's corresponding assigned row and column pixel data making up the image of the object within the selected rows and columns);

however Elabd fails to specifically teach multi-resolution capability having a pixel averaging circuit configured to sample and average pixels within said particular multi-resolution window of claim 1 and first averaging of pixels within each of the plurality of blocks of claim 14. Cho teaches, further limitations of claims 1 and 14, a pixel averaging circuit configured to sample and average pixels within said particular multi-resolution window of claim 1; and first averaging of pixels within each of the plurality of blocks of claim 14 (Column 6, Lines 15-34, where the selected pixels of a block or window of a received light from an image is averaged for purposes of multi resolution vision system, Column 9, Line 64 through Column 10, Line 12);

limitation of claim 3, said multi-resolution window has a size between 1x1 and 32x32 pixels (Column 6, Lines 35-51, where the 3x3 block is within the range);

limitation of claim 4, said pixel averaging circuit includes a plurality of column-parallel capacitors (Column 4, Lines 22-38, where the capacitors are integrated in the column-parallel configuration);

limitation of claims 8 and 15, said pixel averaging circuit includes a super-pixel configuration element that operates to sequentially average the pixels within a super-pixel, where said super-pixel is a group of pixels that is at least 2x2 pixels in size

(Column 6, Lines 28-65, where the block 3x3 pixel image is the super-pixel which is the average value of the selected block);

limitation of claim 16, said first averaging is carried out in a passive capacitor array organized in column-parallel fashion (Column 4, Lines 22-38, where the capacitors are integrated in the column-parallel configuration);

limitation of claim 17, said first averaging includes block-averaging, said block-averaging including: second averaging of a given row of pixel values (Column 6, Lines 56-59, where row average Roweavg(1) is determined); storing an average value (Column 6, Lines 56-59, where row average Roweavg(1) is determined and storing is inherent due to further analysis of the value regarding the block average value determination); repeating said second averaging and storing for all rows, said repeating generating a plurality of row averages (Column 6, Lines 56-65, where the Rowavg for all rows is determined); and computing an average of said plurality of row averages (Column 6, Lines 56-65, the average of all Rowavg is determined according to Column 6, Lines 27-33);

limitation of claim 18, said computing includes switching and hold capacitor in each column (Column 6, Lines 56-65, where switches are controlled according to transfer and blocking of the Rowavg calculations).

It would have been obvious to an ordinary skilled in the art to utilize Cho's averaging technique with Elabd's system because, block averaging would provides light-adaptive sensing mechanism in the imaging device, which is especially desirable in imaging applications under variable lighting conditions (Column 9, Line 66 through Column 10, Line 3).

3. Claims 1-8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (US 5,949,483).

Regarding claims 1-8 and 12, Fossum teaches, limitation of claim 1, a vision system (Column 10, Lines 12-13), comprising: a pixel array having an array of pixels, said array of pixels configured to receive light signals from an image having at least on tracking target (Column 10, Lines 12-27, where a pixel array read out system is discussed, deriving a selected block or the super-pixel block of any size and shape being the target of interest); at least one multi-resolution window operation circuit configured to process said image, each of said at least one multi-resolution window operation circuit operating to process each of said at least one tracking target within a particular multi-resolution window (Column 10, Lines 28-53, where multiresolution blocking or windowing of an image is performed on a selected area of interest being the target area for identification of the area at low or higher resolution as discussed in the same column, Lines 54-67 wherein the low resolution window of the area of an interest or a target area is further transformed into subblocks again to derive the high resolution image of the particular area of the region); and a pixel averaging circuit configured to sample and average pixels within said particular multi-resolution window (Column 10, Lines 28-32, where nine windows of 12x12 pixels are generated from a 36x36 pixel image and where the nine windows of 12x12 windows are further reduced to only a 3x3 or nine pixel windows with each pixel being the average of the previous 12x12 pixel block for low resolution identification of data where the corresponding circuit detail of the above teaching is discussed in Column 11, Lines 3-22, with respect to selection of rows and columns of interest and the averaging circuitry of the generated pixel image data of rows and columns);

Limitation of claim 2, the system further comprising: a target detection circuit configured to receive and process said image such that each of said at least one tracking target is assigned to said particular multi-resolution window (Column 14, Lines 41-53, where from the low resolution processing technique, target or area of interest is identified or detected based on the windowing or blocking operation inherently and the assignment of the identified area or target to the selected or particular block within an image is also inherent);

Limitation of claim 3, said multi-resolution window has a size between 1x1 and 32x32 pixels (Column 10, Lines 28-38, where the multi-resolution window of averaged blocks is a 3x3 pixel block);

Limitation of claim 4, said pixel averaging circuit includes a plurality of column-parallel capacitors (Column 12, Lines 21-16, where capacitors are used for averaging function of column-paralleled configuration of the averaging unit 608 Column 11, Lines 14-22, where the unit 608 is column–parallel configured and utilizes capacitors for it's function);

Limitation of claim 5, system further comprising: at least one output analog signal chain, each of said at least one output analog signal chain configured to output signal from said particular multi-resolution window (Column 11, Lines 33-40, where the output of each of the averaging units 610 averaging a window or a block of particular 3x3 pixels and outputting the results in chain or serial output configuration or in parallel configuration);

Limitation of claim 6, system further comprising: a plurality of latches, each latch configured to hold definition values of said particular multi-resolution window (Column 11, Lines 54-65, where the temporal averaging section 611 is the corresponding latch to

hold the averaged row pixel values for further averaging before outputting to the multiplexer 612);

Limitation of claim 7, each of said array pixels includes a poly-pixel gate biased in deep-depletion (Column 7, Line 47 through Column 8, Line 9, where a polymer is used on silicon base on pixels making it a poly-silicon gate biased in deep-depletion such as permanent deep depletion of red, green and blue filtering of the pixels);

Limitation of claim 8, said pixel averaging circuit includes a super-pixel configuration element that operates to sequentially average the pixels within a super-pixel, where said super-pixel is a group of pixels that is at least 2x2 pixels in size (Column 10, Lines 28-32);

Limitation of claim 12, the system further comprising: row and column control circuits operating to appropriately arrange said light signal received by said pixel array (Column 11, Lines 14-32, where the row and column control is the selection circuitry 606);

However, Fossum does not specifically teach the target being the tracking target being the blocks of data that are averaged and identified based on the received lights from rows and columns of a pixel array of from an image. Fossum clearly suggests utilizing the invention in target tracking environment also (Column 2, lines 15-23). Therefore, it would have been obvious to an ordinary skilled in the art to utilize the fossum's invention in target tracking system because, availability of varying resolution image data allows the user to obtain a unit, e.g., a frame of data at the lowest resolution necessary for the current task that may eliminate unnecessary processing steps associated with obtaining a more detailed image.

Note: Applicant is advised that while the filing data of Fossum et al. reference qualifies as prior art under 102(e), this reference also qualifies as prior art under 102(a) and therefore can not be excluded under 103(c).

Allowable Subject Matter

4. Claims 9-11 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record specifically any of the prior art discussed above does not teach super-pixel average address generation circuit configured to generate addresses of pixels within said super-pixel and mask generation circuit for providing mask pattern for averaging pixels of claim 9 combined with other features and elements of the claim.

Other prior art cited

5. Prior art of record cited and not relied upon is considered pertinent to applicant's disclosure.

The US Patent 6,455,831; US Patent 6,434,254; US Patent 5,961,571; US Patent 5,644,386 and US Patent 5,323,987 variously teach target detection and tracking techniques related to applicant's invention as claimed.

Contact information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shervin Nakhjavan whose telephone number is (703) 306-5916. The examiner can normally be reached on Monday through Friday from 8:00 am to 5:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Boudreau, can be reached at (703) 305-4706.

Any response to this action should be mailed to:
Assistant Commissioner for Patents

Washington, DC 20231

Or faxed to:

(703) 872-9306 for ***formal*** communications, please mark **"EXPEDITED PROCEDURE"**

or:

for ***informal*** or ***draft*** communications; please label "**PROPOSED**" or "**DRAFT**".

Hand delivered responses should be brought to Crystal Park 2, 2121 Crystal drive, Arlington, VA, sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Tech center 2700 customer service office **(703) 306-0377**.

Shervin Nakhjavan S.N
Patent Examiner
Group Art Unit 2621
December 18, 2003.

ANDREW W. JOHNS
PRIMARY EXAMINER